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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	**Application No.** 10/082,776	**Applicant(s)** BENNETT ET AL.
	Examiner Aimee J. Li	**Art Unit** 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been considered. Claims 1, 2, 6, 8, 13, 15, and 20 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 07 November 2006.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The independent claims 1, 8, and 15 have been amended to recite limitations regarding the "pipeline latency". When reviewing the specification, the Examiner located the following definition on page 22, end of paragraph 0047: "For purposes of the present invention, 'pipeline latency' is the rate at which data or a thread traverses a multi-thread execution pipeline loop." Then on pages 25-26, paragraph 0053 there are two more specific definitions of "pipeline latency", which were dependent upon the embodiment of the invention, followed by the conclusion statement "Of course, however, other methods of defining a pipeline latency are well within the scope of the present invention." It is unclear whether any of the definitions for "pipeline latency" are to be read upon the claim language due to the concluding sentence, and, if any of the definitions are to be applied, which definition. Since each embodiment seems to have a separate definition, e.g. pipeline stage execution time vs. full pipeline execution time, that fall

under the general definition given in paragraph 0047, it is unclear to the Examiner which definition, if any, the claim language is referring to. The claim language, taking claim 1 as exemplary, states "said thread sequencing through said entire miss fulfillment FIO before exiting therefrom at a rate having a period associated with said pipeline latency." This claim language has two different interpretations: the phrase regarding the rate modifies the sequencing or the phrase regarding the rate modifies the exiting. Should the phrase regarding the rate modify the sequencing, then the definition with the pipeline latency being the time allowed for each pipeline stage would make sense, but the definition with the pipeline latency being the time for the entire pipeline to be traversed would not make sense and would not be disclosed within the specification, thereby lacking written description. Should the phrase regarding the rate modify the exiting, then the definition with the pipeline latency being the time allowed for each pipeline stage would not make sense and would not make sense, thereby lacking written description, but the definition with the pipeline latency being the time for the entire pipeline to be traversed would make sense. For these reasons, the claim language is unclear.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 6-10, 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Yamin Li and

Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" ©1995 IEEE (herein referred to as Li).

7. Referring to claim 1, Parady has taught a context switching system for a multi-thread execution pipeline loop having a pipeline latency, comprising:

a. A context switch requesting subsystem configured to:

i. Detect a device request from thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

ii. Generate a context Switch request for said thread (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3); and

b. A context controller subsystem configured to receive said context switch request (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

8. Parady has not explicitly taught

a. A miss fulfillment first-in-first-out buffer (FIFO); and

b. Based thereon, store said thread in said miss fulfillment FIFO to prevent said thread from executing until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom at a rate having a period associated with said pipeline latency.

9. However, Parady has taught using a round robin scheduling method (Parady column 4, lines 9-11). Li has taught round robin scheduling (Li page 319, Section 2 A FPMP Architecture, paragraph 4) with a

a. A miss fulfillment first-in-first-out buffer (FIFO) (Li page 320, Section 2 A FPMP Architecture, paragraph 6); and

b. Based thereon, store said thread in said miss fulfillment FIFO to prevent said thread from executing until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom at a rate having a period associated with said pipeline latency (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

10. In regards to Li, the Instruction Scheduling Unit has FIFO registers for each instruction slot, so that unused instructions, e.g. instructions which are not issued to the execution pipelines, are stored until the next cycle, e.g. next time instructions are issued to the execution pipelines. In Li's pipeline a clock cycle is equivalent to the pipeline latency, since it is the number of cycles each stage in the pipeline takes to complete its specific task. The FIFO holds the un-issued instructions until the next clock cycle and the oldest instruction in the FIFO registers for an instruction slot is issued first while the rest of the instructions in the FIFO are moved to the next register in the FIFO until it reaches the head of the FIFO, where it is issued to the execution pipelines if it is ready the next clock cycle. One of Li's considerations to determine whether an instruction is ready to issue is whether all of the source operands are available (Li page 319, Section 2 A FPMP Architecture, paragraph 5). If not all the operands are available for an instruction, the instruction is not issued, so it is held in the FIFO where all the un-issued

instructions for that instruction slot are held until they can be issued in order. Therefore, the FIFO in the ISU is similar to the claimed FIFO, since the thread instructions whose operands are not available are stored in the FIFO and the FIFO sequences the instructions in it every clock cycle, e.g. the pipeline latency, until it the instruction is issued. A person of ordinary skill in the art at the time the invention was made, and as taught by Li, would have recognized that the round robin scheduling scheme and FIFO to store un-issued thread instructions gives each thread equal opportunity to be scheduled and prevents incorrect data from entering the pipeline (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 4-6), thereby preventing thread starvation and ensuring correct data execution. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the scheduling of Li in the device of Parady to prevent thread starvation and ensure correct data execution.

11. Referring to claim 8, Parady has taught for use with a multi-thread execution pipeline loop having a pipeline latency, a method of operating a context switching system, comprising:

a. Detecting a device request from a thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3);

b. Generating a context switch request for said thread when said thread issues said device request (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3); and

c. Receiving said context switch request (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

12. Parady has not explicitly taught storing said thread based thereon in a miss fulfillment first-in-first-out buffer (FIFO) until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom. However, Parady has taught using a round robin scheduling method (Parady column 4, lines 9-11). Li has taught round robin scheduling (Li page 319, Section 2 A FPMP Architecture, paragraph 4) and storing said thread based thereon in a miss fulfillment first-in-first-out buffer (FIFO) until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom at a rate associated with said pipeline latency (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6). In regards to Li, the Instruction Scheduling Unit has FIFO registers for each instruction slot, so that unused instructions, e.g. instructions which are not issued to the execution pipelines, are stored until the next cycle, e.g. next time instructions are issued to the execution pipelines. In Li's pipeline a clock cycle is equivalent to the pipeline latency, since it is the number of cycles each stage in the pipeline takes to complete its specific task. The FIFO holds the un-issued instructions until the next clock cycle and the oldest instruction in the FIFO registers for an instruction slot is issued first while the rest of the instructions in the FIFO are moved to the next register in the FIFO until it reaches the head of the FIFO, where it is issued to the execution pipelines if it is ready the next clock cycle. One of Li's considerations to determine whether an instruction is ready to issue is whether all of the source operands are available (Li page 319, Section 2 A FPMP Architecture, paragraph 5). If not all the

operands are available for an instruction, the instruction is not issued, so it is held in the FIFO where all the un-issued instructions for that instruction slot are held until they can be issued in order. Therefore, the FIFO in the ISU is similar to the claimed FIFO, since the thread instructions whose operands are not available are stored in the FIFO and the FIFO sequences the instructions in it every clock cycle, e.g. the pipeline latency, until it the instruction is issued. A person of ordinary skill in the art at the time the invention was made, and as taught by Li, would have recognized that the round robin scheduling scheme and FIFO to store un-issued thread instructions gives each thread equal opportunity to be scheduled and prevents incorrect data from entering the pipeline (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 4-6), thereby preventing thread starvation and ensuring correct data execution. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the scheduling of Li in the device of Parady to prevent thread starvation and ensure correct data execution.

13. Referring to claims 2 and 9, Parady in view of Li has taught wherein said context controller subsystem is further configured to allow a new thread to enter said multi-thread execution pipeline loop after storing said thread in said miss fulfillment FIFO (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

14. Referring to claims 3 and 10, Parady in view of Li has taught wherein said context controller subsystem is further configured to allow other threads within said multi-thread execution pipeline loop to continue to execute while said thread is waiting for said device request to be fulfilled (Parady column 2, lines 28-34; column 3, line 57 to column 4, line 18; column 4, line 42-62; and Figure 3).

15. Referring to claims 4 and 11, Parady in view of Li has taught wherein said context controller subsystem is further configured to:

a. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6), and

b. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position after said thread exits said miss fulfillment FIFO (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

16. Referring to claims 5 and 12, Parady in view of Li has taught wherein said thread is looped back to a beginning stage of said multi-thread execution pipeline loop when said thread reaches an end stage of said multi-thread execution pipeline loop and said thread has not finished processing (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

17. Referring to claims 6 and 13, Parady in view of Li has taught wherein said context controller subsystem is further configured to sequence said thread through said miss fulfillment FIFO at a rate equal to said pipeline latency of said multi-thread execution pipeline loop (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

18. Referring to claims 7 and 14, Parady in view of Li has taught wherein said device request is a request to access external memory due to a cache miss status (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

19. Claims 15-17 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Wilford et al.,

U.S. Patent Number 5,509,006 (herein referred to as Wilford) and in further view of Yamin Li and Wanming Chu's "The Effects of STEF in Finely Parallel Multithreaded Processors" ©1995 IEEE (herein referred to as Li).

20. Referring to claim 15, Parady has taught a fast pattern processor that receives and processes protocol data units (PDUs), comprising:

a. A dynamic random access memory (DRAM) that contains instructions (Parady column 5, lines 19-22; Figure 5; and Figure 6). In regards to Parady, DRAM in a specific type of RAM and Parady shows that RAM is used in his system. Please see Rosenberg's <u>Computers, Information Processing & Telecommunications</u> Second Edition for more information of RAM and DRAM.

b. A memory cache that caches certain of said instructions from said DRAM (Parady column 5, lines 19-22; Figure 5; and Figure 6); and

c. An engine that employs said DRAM and said memory cache to obtain ones of said instructions (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), including:

i. A multi-thread execution pipeline loop having a pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

ii. A context switching system for said multi-thread execution pipeline loop (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34;

column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), having:

(1) A context switch requesting subsystem that: detects a device request from a thread executing within said multi-thread execution pipeline loop for access to a device having a fulfillment latency exceeding said pipeline latency (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

(2) Generates a context switch request for said thread (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3), and

iii. A context controller subsystem that receives said context switch request and prevents said thread from executing until said device request is fulfilled (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

21. Parady has not taught a tree engine that parses data within said PDUs. Wilford has taught a tree engine that parses data within said PDUs (Wilford column 1, lines 34-42; column 1, line 65 to column 2, line 19; column 14, lines 14-35; and Figure 5B). A person of ordinary skill in the art at the time the invention was made, and as taught in Wilford, would have recognized that a tree engine that parses data within said PDUs identifies which protocol the data belongs to in

order to send the data to the correct destination (Wilford column 1, lines 34-42), thereby ensuring correct data execution. Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the tree engine of Wilford in the device of Parady to ensure correct data execution.

22. In addition, Parady has not explicitly taught

a. A miss fulfillment first-in-first-out buffer (FIFO); and

b. Based thereon, stores said thread in said miss fulfillment FIFO until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom.

23. However, Parady has taught using a round robin scheduling method (Parady column 4, lines 9-11). Li has taught round robin scheduling (Li page 319, Section 2 A FPMP Architecture, paragraph 4) with a

a. A miss fulfillment first-in-first-out buffer (FIFO) (Li page 320, Section 2 A FPMP Architecture, paragraph 6); and

b. Based thereon, store said thread in said miss fulfillment FIFO to prevent said thread from executing until said device request is fulfilled, said thread sequencing through said entire miss fulfillment FIFO before exiting therefrom at a rate having a period associated with said pipeline latency (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

24. In regards to Li, the Instruction Scheduling Unit has FIFO registers for each instruction slot, so that unused instructions, e.g. instructions which are not issued to the execution pipelines, are stored until the next cycle, e.g. next time instructions are issued to the execution pipelines. In

Li's pipeline a clock cycle is equivalent to the pipeline latency, since it is the number of cycles each stage in the pipeline takes to complete its specific task. The FIFO holds the un-issued instructions until the next clock cycle and the oldest instruction in the FIFO registers for an instruction slot is issued first while the rest of the instructions in the FIFO are moved to the next register in the FIFO until it reaches the head of the FIFO, where it is issued to the execution pipelines if it is ready the next clock cycle. One of Li's considerations to determine whether an instruction is ready to issue is whether all of the source operands are available (Li page 319, Section 2 A FPMP Architecture, paragraph 5). If not all the operands are available for an instruction, the instruction is not issued, so it is held in the FIFO where all the un-issued instructions for that instruction slot are held until they can be issued in order. Therefore, the FIFO in the ISU is similar to the claimed FIFO, since the thread instructions whose operands are not available are stored in the FIFO and the FIFO sequences the instructions in it every clock cycle, e.g. the pipeline latency, until it the instruction is issued. A person of ordinary skill in the art at the time the invention was made, and as taught by Li, would have recognized that the round robin scheduling scheme and FIFO to store un-issued thread instructions gives each thread equal opportunity to be scheduled and prevents incorrect data from entering the pipeline (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 4-6), thereby preventing thread starvation and ensuring correct data execution. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the scheduling of Li in the device of Parady to prevent thread starvation and ensure correct data execution.

25. Referring to claim 16, Parady in view of Wilford and in further view of Li has taught wherein said context controller subsystem further allows a new thread to enter said multi-thread

execution pipeline loop after storing said thread in said FIFO (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

26. Referring to claim 17, Parady in view of Wilford and in further view of Li has taught wherein said context controller subsystem further allows other threads within said multi-thread execution pipeline loop to continue to execute while said thread is waiting for said device request to be fulfilled (Parady column 2, lines 28-34; column 3, line 57 to column 4, line 18; column 4, line 42-62; and Figure 3).

27. Referring to claim 18, Parady in view of Wilford and in further view of Li has taught wherein said context controller subsystem is further configured to:

d. Store said thread in said miss fulfillment FIFO upon reaching an end position of said multi-thread execution pipeline loop (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6), and

e. Reinsert said thread into said multi-thread execution pipeline loop at a beginning position after said thread exits said miss fulfillment FIFO (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

28. Referring to claim 19, Parady in view of Wilford and in further view of Li has taught wherein said thread is looped back to a beginning stage of said multi-thread execution pipeline loop when said thread reaches an end stage of said multi-thread execution pipeline loop and said thread has not finished processing (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

29. Referring to claim 20, Parady in view of Wilford and in further view of Li has taught wherein said context controller subsystem further sequences said thread through said miss

fulfillment FIFO at a rate equal to said pipeline latency of said multi-thread execution pipeline loop (Li pages 319-320, Section 2 A FPMP Architecture, paragraphs 3-6).

30. Referring to claim 21, Parady in view of Wilford and in further view of Li has taught wherein said device request is said DRAM and said device request is a request to access said DRAM due to a cache miss status from said memory cache (Parady Abstract; column 1, lines 29-35 and 46-57; column 2, lines 18-34; column 3, line 57 to column 4, line 18; column 4, lines 42-62; Figure 3).

Response to Arguments

31. Applicant's arguments with respect to claims 1-21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Eickemeyer et al., U.S. Patent Application Publication 2003/0005263; U.S. Patent Number 6,988,186; U.S. Patent Number 6,931,639; and U.S. Patent Number 6,694,425 have taught instruction issue queues in a multi-threaded system.

b. Dirceu Cavendish's "CORPS – A Pipelined Fair Packet Scheduler for High Speed Switches" ©June 2000 IEEE has taught a round robin scheduling scheme with issue queues.

33. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

34. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Aimee J. Li
20 January 2007

Eddie Chan

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